
# A Routed Clock Skew Analysis on Actel's A54SX32A and RTSX32SU Products

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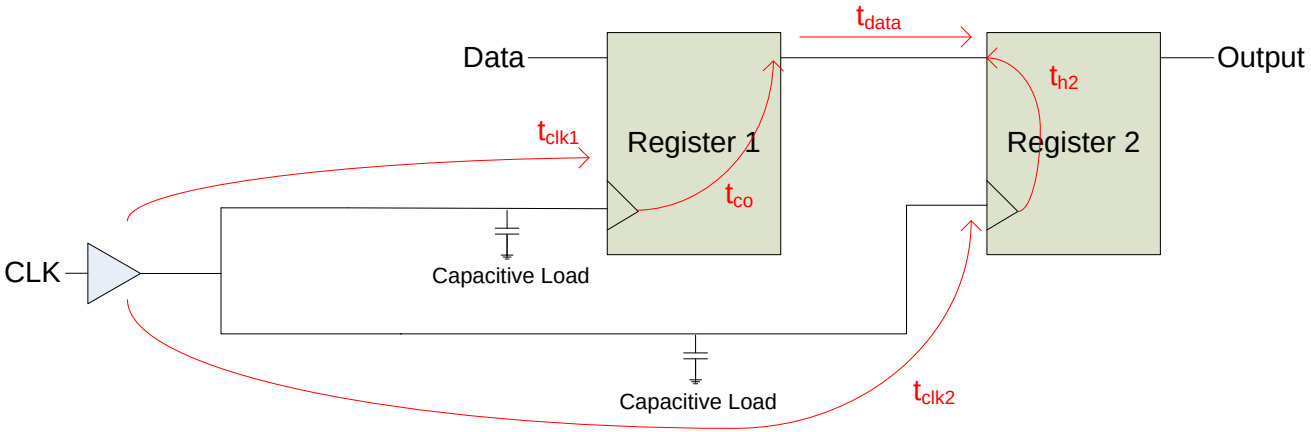
# Outline

- Introduction
- Global Architecture
- Experiment Strategy
- Experiment Results
- Additional Details
- Conclusion

# Introduction

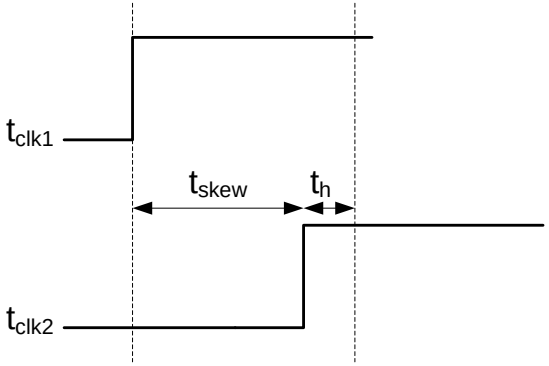
- Issue
  - **An extreme case using RCLK saw clock skew contributing to a hold-time violation**
- Goal
  - **Investigate the situation for clock-skew induced hold time violations on the routed clocks in Actel A54SX32A/RTSX32SU devices**
- Experiment
  - **Using a design with an extreme topology and tweaked Actel software, devices from different wafer lots at full range of temperature and voltage operating conditions were tested to determine the susceptibility of the routed clock to a skew-induced failure**

# Introduction: Hold Time



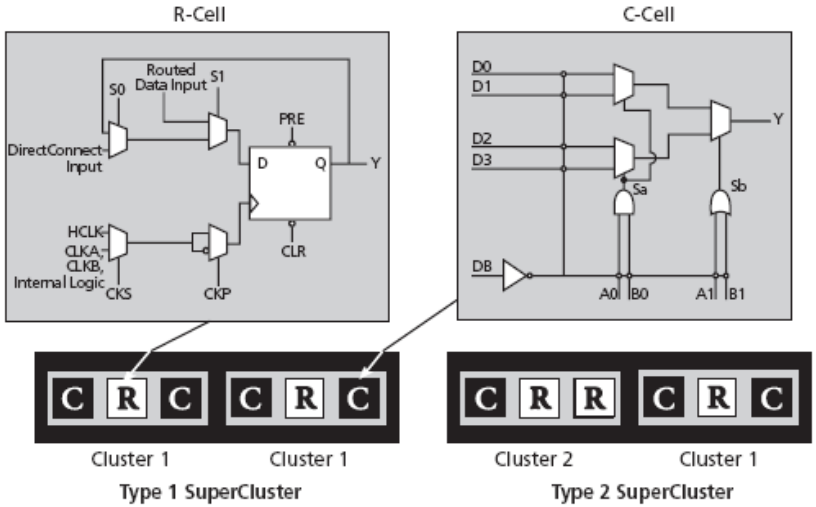

## Passing Condition:

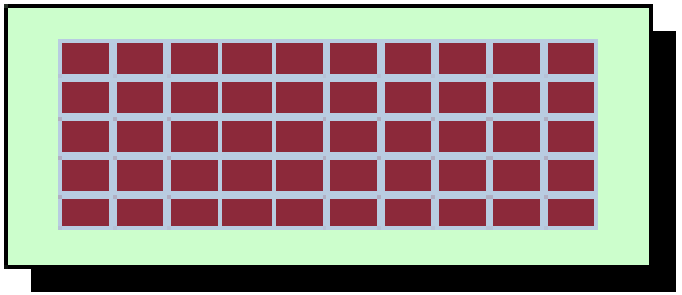
$$t_{co} + t_{data} > t_{skew} + t_{h2}$$



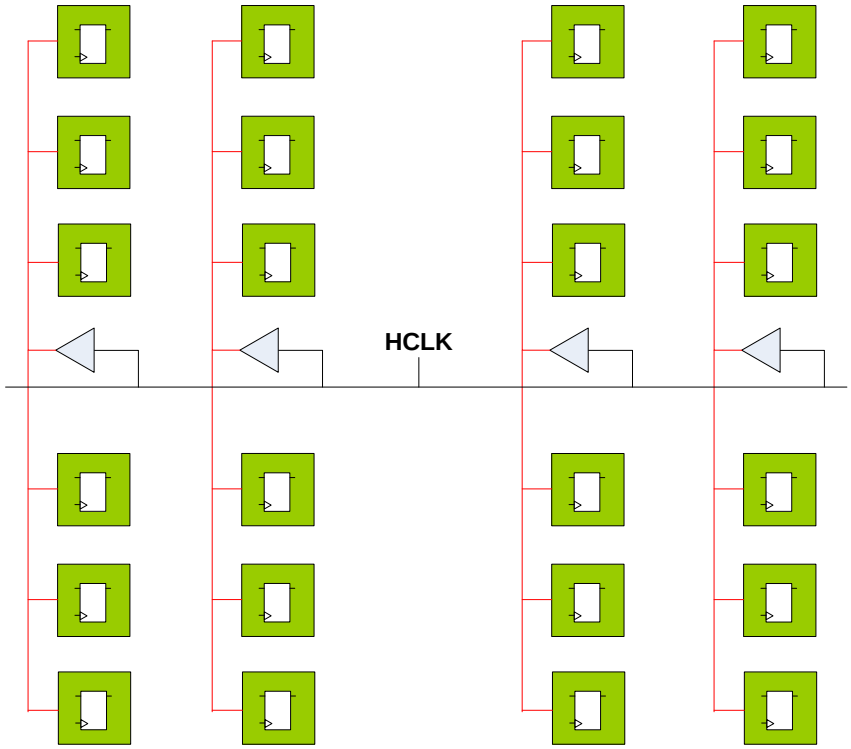
# Architecture: Logic Modules

- "Sea-of-Modules"
  - **Register/Sequential Cell (R-cell)**
    - **Clock source can be hardwired clock, routed clock, or internal logic**
  - **Combinational Cell (C-Cell)**
    - **Hardwired clock cannot be used as clock source**
- A54SX32A Module Capacity
  - **Register/Sequential Cell (R-cell)**
    - **1080 modules**
  - **Combinational Cell (C-cell)**
    - **1800 modules**
    - **2 C-cells may be configured as a flip-flop**

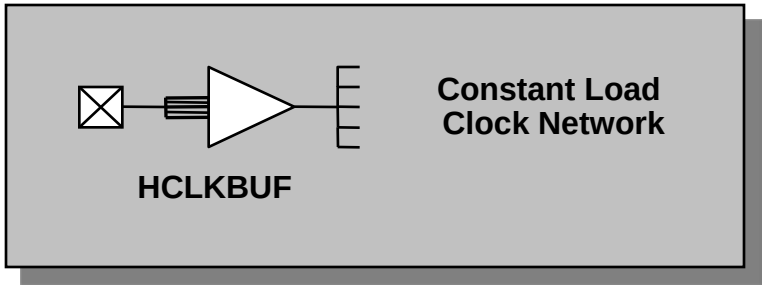


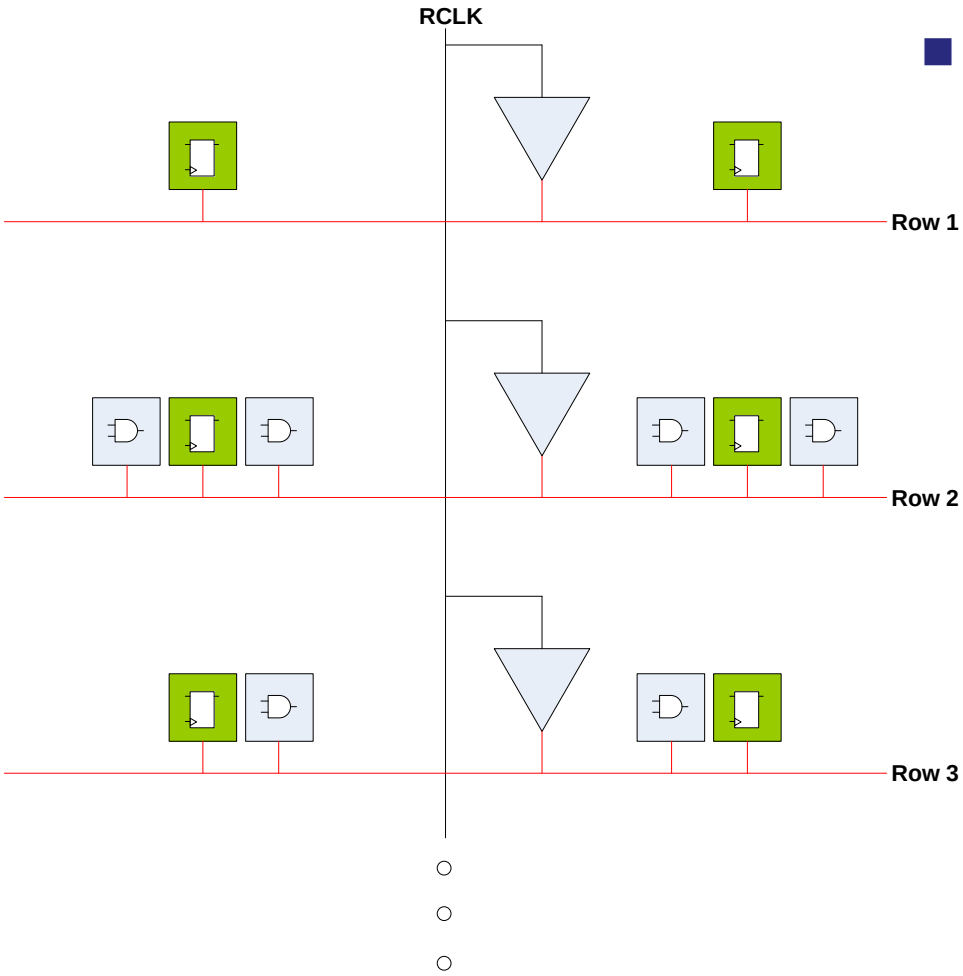
# Architecture: Simplified HCLK Structure



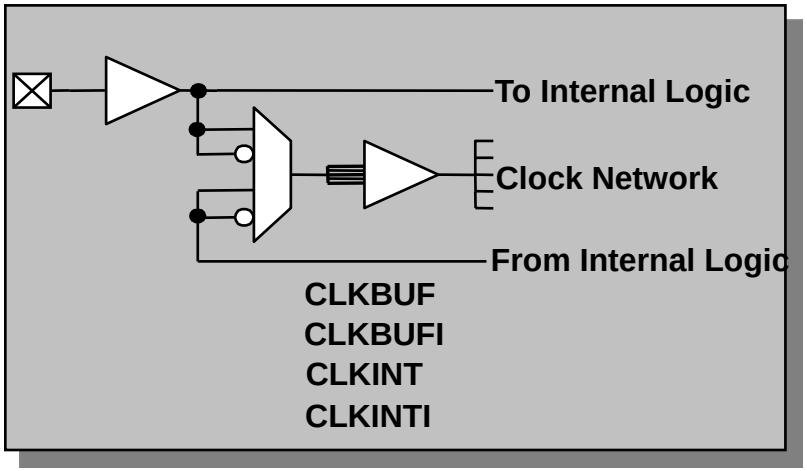

- Hardwired Clock (HCLK)
  - **Hardwired directly to the clock inputs of Sequential Cells**
  - **Cannot connect to C-Cells – only R-Cells**
  - **No programming elements in path**
  - **Negligible, fixed skew**
  - **Immune to violation**



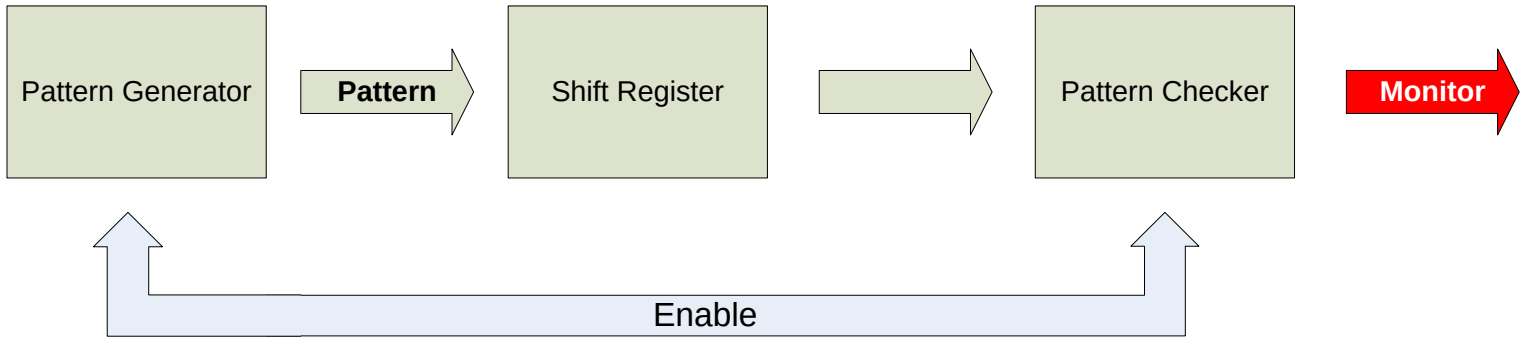
# Architecture: Simplified RCLK Structure




- Routed Clock (RCLK)
  - **More flexible: can connect to both R-Cells and C-Cells**
  - **Limited but variable skew dependent upon distribution of loads on clock network**

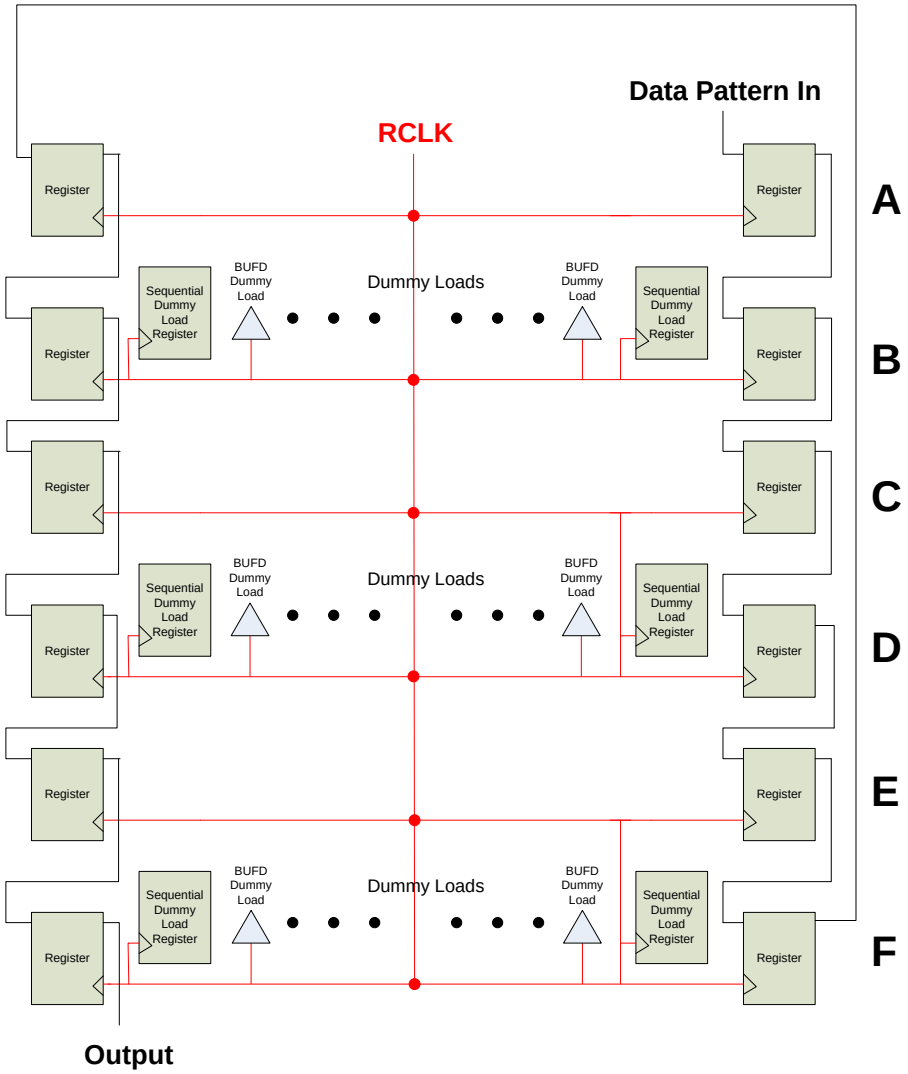


# Experiment Details




- Pattern Generator
- Shift Register
- Pattern Checker

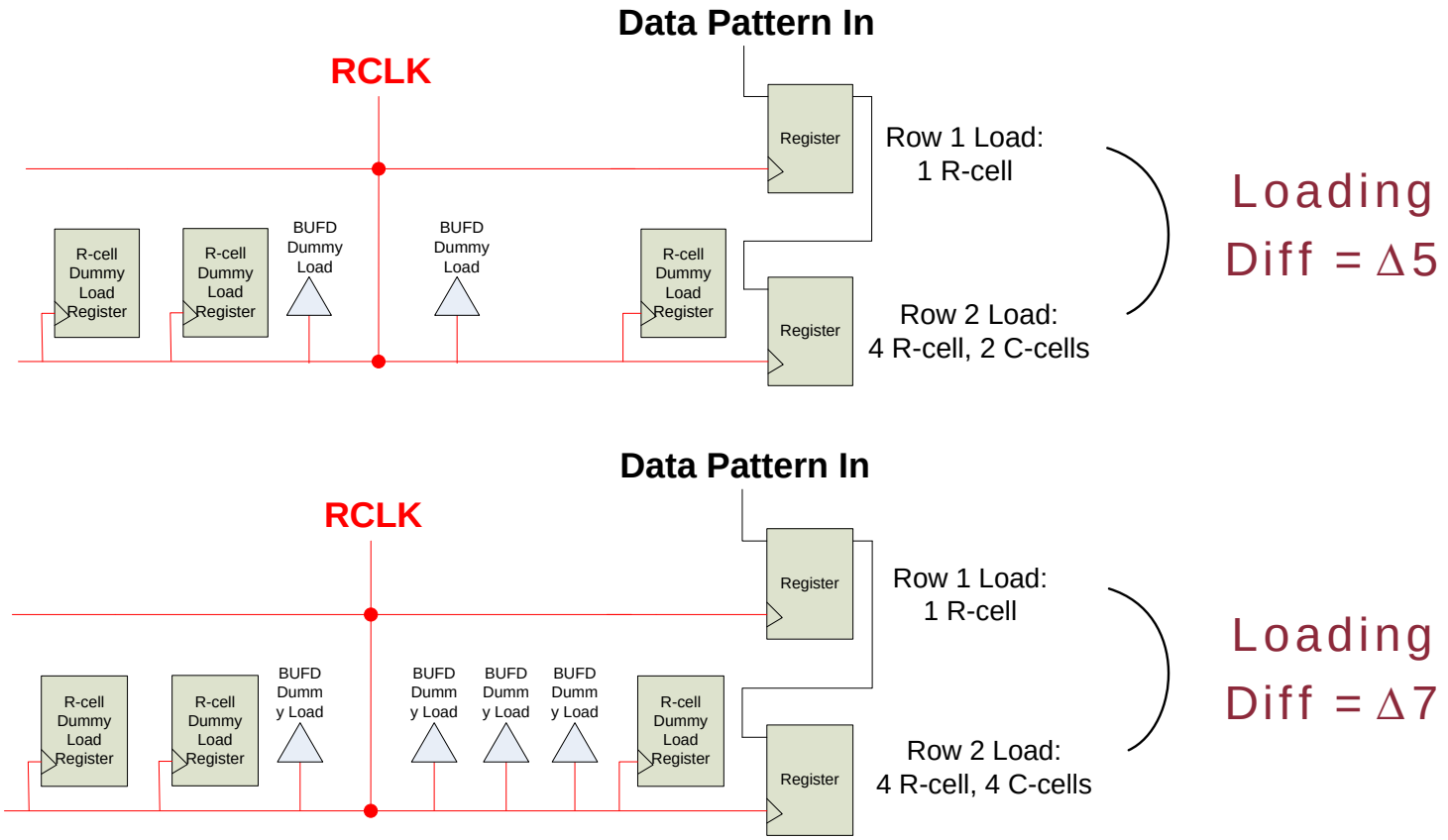
# Shift Register Test Design




- Shift Register
  - Alternating rows of lightly-loaded to heavily-loaded rows
  - Worst case is transition from lightly-loaded to heavily-loaded RCLK segments (A → B)
  - Shortest possible data paths
  - Manually placed

# Loading Difference Examples

- Simplified Examples:



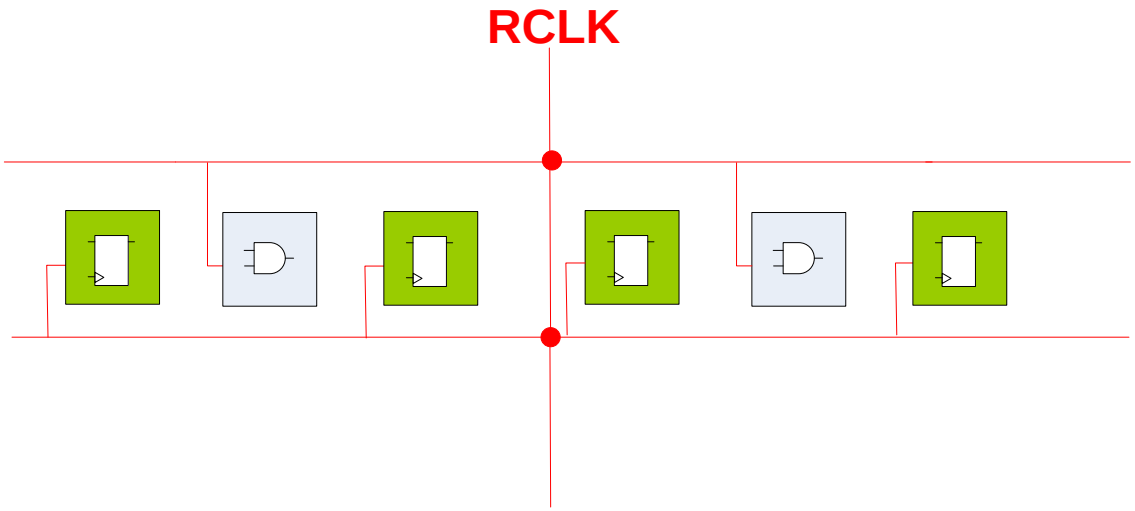

- Used in experiment: A54SX32A/RTSX32SU load difference = 34 Sequential + X BUFDs

# Test Results Summary

- Tested over 100 devices with varying temperature/voltage conditions
- A54SX32A devices:
  - **Safe margin up to: 34 R-cells (all R-Cells used) + 7 BUFDs (C-Cells) = load delta of 41**
- RTSX32SU devices:
  - **Safe margin up to: 34 R-cells (all R-Cells used) + 18 BUFDs (C-Cells) = load delta of 52**
- These load deltas cannot be reached if only R-cells are used

# Additional Safety Margin

- Built-In load balancing by Actel software
  - **Disabled in experiment via software modification**

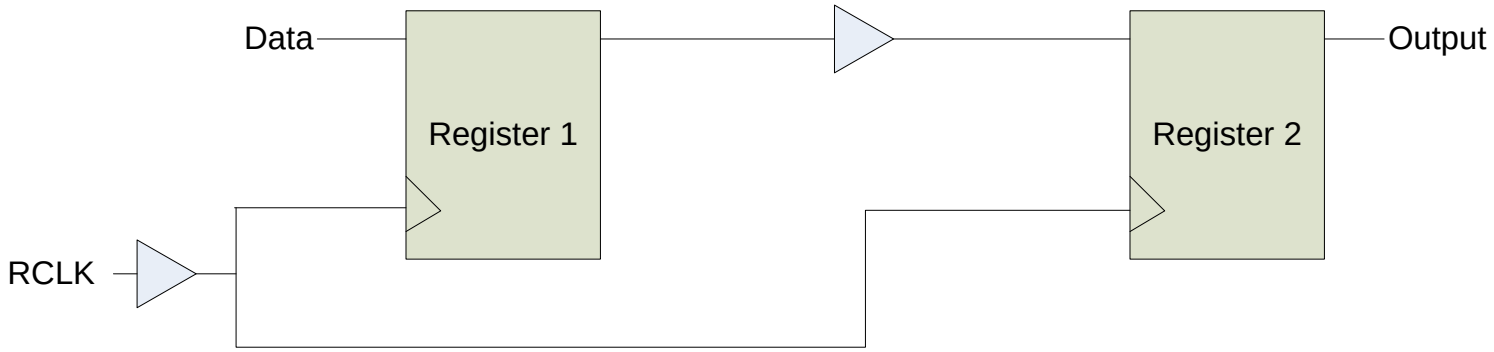



- Sequential Cells
  - **Utilizes the lower RCLK segment**
- Combinational Cells
  - **Can individually use either higher or lower segment for better load balancing**

# Additional Safety Margin

## KBI (K-Antifuse Buffer Insertion) in Actel software

- **Inserts buffer in between registers to slow down data path**




## KBI Disabled in Experiment

- **KBI disabled in Actel software for fastest data path**

# Conclusion

- A54SX32A/RTSX32SU RCLK is totally immune to hold time violations if loaded exclusively with sequential elements
- Built-in software features provide additional margin